WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a substrate;

a nonvolatile memory device formed in a memory cell region of said substrate and having a multilayer gate electrode structure comprising a tunnel insulating film covering said substrate and a floating gate electrode formed on the tunnel insulating film and having sidewall surfaces covered with a protection insulating film formed of a thermal oxide film; and

a semiconductor device formed in a device region of said substrate, the semiconductor device comprising a gate insulating film covering said substrate and a gate electrode formed on the gate insulating film,

wherein a bird's beak structure is formed of a thermal oxide film at an interface of the tunnel insulating film and the floating gate electrode, the bird's beak structure penetrating into the floating gate electrode along the interface from the sidewall faces of the floating gate electrode; and

the gate insulating film is interposed between said substrate and the gate electrode to have a substantially uniform thickness.

2. The semiconductor integrated circuit device as claimed in claim 1, wherein the multilayer

gate electrode structure further comprises an insulating film formed on the floating gate electrode and a control gate electrode formed on the insulating film.

3. The semiconductor integrated circuit device as claimed in claim 2, wherein each of the gate electrode and the control gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

4. The semiconductor integrated circuit device as claimed in claim 1, wherein the thermal oxide film forming the protection insulating film connects to the bird's beak structure.

5. The semiconductor integrated circuit device as claimed in claim 1, wherein the protection insulating film continuously covers sidewall faces and a top surface of the multilayer gate electrode structure.

6. The semiconductor integrated circuit device as claimed in claim 1, wherein a silicon-on-

insulator substrate is employed as said substrate.

7. The semiconductor integrate circuit device as claimed in claim 1, wherein the tunnel insulating film is a tunnel oxide film.

8. The semiconductor integrate circuit device as claimed in claim 1, wherein the tunnel insulating film is a tunnel nitride film.

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9. A semiconductor integrated circuit device comprising:

a substrate;

a nonvolatile memory device formed in a memory cell region of said substrate,

the nonvolatile memory device comprising:

a first active region covered with a tunnel insulating film;

a second active region formed next to the first active region and covered with an insulating film;

a control gate formed of an embedded diffusion region formed in the second active region;

a first gate electrode extending on the tunnel insulating film in the first active region and forming a bridge between the first and second active regions to be capacitive-coupled via the insulating film to the embedded diffusion region

in the second active region, the first gate electrode having sidewall faces thereof covered with a protection insulating film formed of a thermal oxide film; and

a diffusion region formed on each of sides of the first gate electrode in the first active region; and

a semiconductor device formed in a device region of said substrate, the semiconductor device comprising a gate insulating film covering said substrate and a second gate electrode formed on the gate insulating film,

wherein a bird's beak structure is formed of a thermal oxide film at an interface of the tunnel insulating film and the first gate electrode, the bird's beak structure penetrating into the first gate electrode along the interface from the sidewall faces of the first gate electrode; and

the gate insulating film is interposed between said substrate and the second gate electrode to have a substantially uniform thickness.

10. The semiconductor integrated circuit device as claimed in claim 9, wherein the thermal oxide film forming the protection insulating film is connected to the bird's beak structure.

11. The semiconductor integrated circuit device as claimed in claim 9, wherein the protection insulating film continuously covers a top surface of the first gate electrode.

12. The semiconductor integrated circuit device as claimed in claim 9, wherein the second gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

13. The semiconductor integrated circuit device as claimed in claim 9, wherein a silicon-on-insulator substrate is employed as said substrate.

14. The semiconductor integrated circuit device as claimed in claim 9, wherein the tunnel insulating film is a tunnel oxide film.

15. The semiconductor integrated circuit device as claimed in claim 9, wherein the tunnel insulating film is a thermal nitride oxide film.

16. A method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a semiconductor structure including a tunnel insulating film covering a memory cell region of a substrate, a first silicon film covering the tunnel insulating film, an insulating film covering the first silicon film, and a gate

insulating film covering a logic device region of the substrate;

(b) depositing a second silicon film on the semiconductor structure formed in said step (a) so that the second silicon film covers the insulating film in the memory cell region and the gate insulating film in the logic device region;

(c) forming a multilayer gate electrode structure in the memory cell region by successively patterning the second silicon film to serve as a control gate electrode, the insulating film, and the first silicon film in the memory cell region with the second silicon film being left in the logic device region;

(d) forming a protection oxide film so that the protection oxide film covers the multilayer gate electrode structure in the memory cell region and the second silicon film in the logic device region;

(e) forming diffusion regions in both sides of the multilayer gate electrode structure in the memory cell region by performing ion implantation of an impurity element into the substrate with the multilayer gate electrode structure and the second silicon film being employed as masks;

(f) forming a gate electrode in the logic device region by patterning the second silicon film; and

(g) forming diffusion regions in the logic device region by performing ion implantation with the gate electrode being employed as a mask,

whereby a nonvolatile memory device is formed in the memory cell region and a semiconductor device is formed in the logic device region.

17. The method as claimed in claim 16, wherein the logic device region comprises first and second device regions;

said step (a) forms first and second gate insulating films in the first and second device regions, respectively, the second insulating film being thicker than the first insulating film;

said step (f) forms first and second gate electrodes in the first and second device regions, respectively, by patterning the second silicon film; and

said step (g) forms diffusion regions in the first and second device regions by employing the first and second gate electrodes being employed as masks, respectively.

18. The method as claimed in claim 17, wherein said step (b) is performed simultaneously in the memory cell region and the first and second device regions.

19. The method as claimed in claim 17, wherein each of the control gate electrode and the first and second gate electrodes comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

20. The method as claimed in claim 16,

wherein said step (b) is performed simultaneously in the memory cell region and the logic device region.

21. The method as claimed in claim 16, wherein said step (e) is performed without using a resist mask.

22. The method as claimed in claim 16, wherein said step (a) employs a tunnel oxide film as the tunnel insulating film.

23. The method as claimed in claim 16, wherein said step (a) employs a tunnel nitride film as the tunnel insulating film.

24. The method as claimed in claim 16, wherein a silicon-on-insulator substrate is employed as the substrate.

25. The method as claimed in claim 16, wherein said step (d) forms the protection oxide film by thermal oxidation so that the protection

oxide film is formed of a thermal oxide film.

26. The method as claimed in claim 16, wherein said step (g) performs ion implantation with the memory cell region being protected by a resist mask.

27. The method as claimed in claim 16, wherein each of the control gate electrode and the gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

28. A method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a semiconductor structure comprising a tunnel insulating film covering a memory cell region of a substrate and a gate insulating film covering a logic device region of the substrate;

(b) depositing a silicon film on the semiconductor structure formed in said step (a) so that the silicon film covers the tunnel insulating film in the memory cell region and the gate insulating film in the logic device region;

(c) forming a first gate electrode in the memory cell region by selectively patterning the silicon film with the silicon film being left in the

logic device region;

(d) forming a protection oxide film so that the protection oxide film covers the first gate electrode in the memory cell region and the silicon film in the logic device region;

(e) forming diffusion regions on both sides of the first gate electrode in the memory cell region by performing ion implantation of an impurity element into the substrate with the first gate electrode and the silicon film being employed as masks;

(f) forming a second gate electrode in the logic device region by patterning the silicon film; and

(g) forming diffusion regions in the logic device region by performing ion implantation with the second gate electrode being employed as a mask,

whereby a nonvolatile memory device is formed in the memory cell region and a semiconductor device is formed in the logic device region.

29. The method as claimed in claim 28, wherein the logic device region comprises first and second device regions;

said step (a) forms first and second gate insulating films in the first and second device regions, respectively, the second insulating film being thicker than the first insulating film;

said step (f) forms third and fourth gate electrodes in the first and second device regions, respectively, by patterning the second silicon film; and

said step (g) forms diffusion regions in the first and second device regions by employing the

third and fourth gate electrodes being employed as masks, respectively.

30. The method as claimed in claim 29, wherein said step (b) is performed simultaneously in the memory cell region and the first and second device regions.

31. The method as claimed in claim 29, wherein each of the third and fourth gate electrodes comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.

32. The method as claimed in claim 28, wherein said step (b) is performed simultaneously in the memory cell region and the logic device region.

33. The method as claimed in claim 28, wherein said step (e) is performed without using a resist mask.

34. The method as claimed in claim 28, wherein said step (a) employs a tunnel oxide film as the tunnel insulating film.

35. The method as claimed in claim 28, wherein said step (a) employs a tunnel nitride film as the tunnel insulating film.

36. The method as claimed in claim 28, wherein a silicon-on-insulator substrate is employed as the substrate.

37. The method as claimed in claim 28, wherein said step (d) forms the protection oxide film by thermal oxidation so that the protection oxide film is formed of a thermal oxide film.

38. The method as claimed in claim 28, wherein said step (g) performs ion implantation with the memory cell region being protected by a resist mask.

39. The method as claimed in claim 28, wherein the second gate electrode comprises a polycide or polymetal structure including a silicon film doped with an n-type or p-type dopant.